

***Amendments to the Claims***

This listing of claims will replace all prior versions, and listings of claims in the application.

1-16. *(Canceled)*

17. *(New)* A method of mapping a series of digital levels to a series of corresponding pulses, comprising the steps of:

- (1) defining a first pulse having a first time domain centroid and a second pulse having a second time domain centroid that is different from the first time domain centroid, wherein said first pulse and said second pulse correspond to a digital level of said series of digital levels;
- (2) receiving at an input of a circuit a signal corresponding to said digital level;
- (3) selectively providing at an output of the circuit, as an output pulse, either said first pulse or said second pulse in response to receiving said signal; and
- (4) controlling step (3) such that over time a substantially equal number of said first and second pulses is provided at the output of the circuit.

18. *(New)* A method of mapping a series of digital levels to a series of corresponding pulses, comprising the steps of:

- (1) defining at least a first pulse and a second pulse, wherein said first pulse and said second pulse correspond to a digital level of said series of digital levels;
- (2) receiving at an input of a circuit a signal corresponding to said digital level;
- (3) selectively providing at an output of the circuit, as an output pulse, either said first pulse or said second pulse in response to receiving said signal; and
- (4) controlling the step of selectively providing to alternate between said first and second pulses each time said signal is received, wherein said first and second pulses have different time domain centroids.

19. (*New*) A method of mapping a series of digital levels to a series of corresponding pulses, comprising the steps of:

- (1) defining at least first and second pulse sets, each pulse set defining a respective bit sequence corresponding to each digital level of said series of digital levels;
- (2) receiving at an input of a circuit a signal corresponding to a digital level of said series of digital levels;
- (3) selectively providing at an output of the circuit, as an output pulse, either a first pulse defined in said first pulse set or a second pulse defined in said second pulse set; and
- (4) controlling the step of selectively providing such that over time a substantially equal number of said first and second pulses is provided at the

output of the circuit, wherein said first pulse and said second pulse have different time domain centroids.

20. (*New*) The method of claim 19, wherein the controlling step includes alternating between said first pulse and said second pulse.

21. (*New*) The method of claim 19, wherein output pulses are selected from a plurality of pulse sets that includes said first and second pulse sets by alternating among said plurality of pulse sets, for at least those digital levels that correspond with a plurality of different pulses.

22. (*New*) The method of claim 21, wherein pulses in said first pulse set and pulses in said second pulse set have substantially equal time domain centroids.

23. (*New*) The method of claim 21, wherein pulses in each pulse set of said plurality of pulse sets have substantially equal time domain centroids.

24. (*New*) A method of mapping a series of digital levels to a series of corresponding pulses, comprising the steps of:

(1) defining at least first and second pulses, wherein said first and second pulses are pulse width modulated representations of a digital level;

(2) receiving at an input of a circuit a signal corresponding to said digital level and in response, selectively providing at an output of the circuit, as an output pulse, either said first pulse or said second pulse; and

(3) controlling step (2) such that over time a substantially equal number of said first and second pulses is provided at the output of the circuit to represent said digital level when said signal corresponding to said digital level is received at the input of the circuit, based on said first and second pulses having different time domain centroids.

25. (New) A system for mapping a series of digital levels received at an input of a digital modulator circuit to a series of corresponding pulses at an output of the circuit, comprising:

mapping means for defining at least a first pulse having a first bit sequence corresponding to a digital level of said series of digital levels and a second pulse having a second bit sequence corresponding to said digital level, wherein said first and second pulses are different;

pulse generation means for selectively generating either said first pulse or said second pulse as an output pulse at the output of the digital modulator circuit; and

control means for controlling said pulse generation means such that over time a substantially equal number of said first and second pulses is provided at the output of the digital modulator circuit.

26. (New) The system of claim 25 wherein said digital modulator circuit is included in a cable television receiver.

27. (New) A system for mapping a series of digital levels received at an input of a circuit to a series of corresponding pulses at an output of the circuit, comprising:

mapping means for defining at least a first pulse having a first bit sequence corresponding to a digital level of said series of digital levels and a second pulse having a second bit sequence corresponding to said digital level, wherein said first and second pulses are different from each other;

pulse generation means for selectively generating either said first pulse or said second pulse as an output pulse at the output of the circuit; and

control means for controlling said pulse generation means such that over time a substantially equal number of said first and second pulses is provided at the output of the circuit, said control means including means for selectively providing either said first pulse or said second pulse by alternating between said first and second pulses each time said digital level is received.

28. (New) A system for mapping a series of digital levels received at an input of a circuit to a series of corresponding pulses at an output of the circuit, comprising:

mapping means for defining at least a first pulse having a first bit sequence corresponding to a digital level of said series of digital levels and a

second pulse having a second bit sequence corresponding to said digital level, wherein said first and second pulses are different;

    pulse generation means for selectively generating either said first pulse or said second pulse as an output pulse at the output of the circuit; and

    control means for controlling said pulse generation means such that over time a substantially equal number of said first and second pulses is provided at the output of the circuit,

    wherein said mapping means further comprises means for defining at least first and second pulse sets, each pulse set defining a bit sequence corresponding to each of a plurality of digital levels.

29. *(New)* The method of claim 28, wherein the controlling means includes means for alternating between said first pulse and said second pulse.

30. *(New)* The method of claim 28, wherein the controlling means includes means for selecting output pulses from a plurality of pulse sets that includes said first and second pulse sets by alternating among said plurality of pulse sets, for at least those digital levels that correspond with a plurality of different pulses.

31. *(New)* The method of claim 30, wherein pulses in said first pulse set and pulses in said second pulse set have substantially equal time domain centroids.

32. *(New)* The method of claim 30, wherein pulses in each pulse set of said plurality of pulse sets have substantially equal time domain centroids.

33. *(New)* A system for mapping a series of digital levels received at an input of a circuit to a series of corresponding pulses at an output of the circuit, comprising:

mapping means for defining at least first and second pulses, each having a respective bit sequence corresponding to a digital level of said series of digital levels;

pulse generation means for selectively generating either said first pulse or said second pulse as an output pulse at the output of the circuit; and

control means for controlling said pulse generation means such that over time a substantially equal number of said first and second pulses is provided at the output of the circuit,

wherein said first and second pulses are different pulse width modulated representations of said digital level.